M/A-COM

# GaAs MMIC VSAT Power Amplifier, 2W 5.9 - 6.4 GHz



#### Features

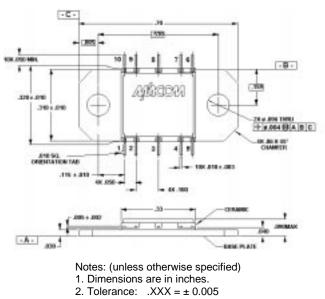
- High Linear Gain: 30 dB Typ.
- High Saturated Output Power: +33 dBm Typ.
- High Power Added Efficiency: 26% Typ.
- 50Ω Input/Output Broadband Matched
- High Performance Ceramic Bolt Down Package

#### Description

M/A-COM's AM42-0040 is a three-stage MMIC power amplifier in a ceramic bolt down style hermetic package. The AM42-0040 employs an internally matched monolithic chip with internally decoupled Gate and Drain bias networks. The AM42-0040 is designed to be operated from a constant current Drain supply. By varying the Gate bias voltage, the saturated output power performance of this device can be tailored for various applications.

The AM42-0040 is designed for use as an output stage or driver amplifier for C-band VSAT transmitter systems. This amplifier employs a fully monolithic chip and requires a minimum of external components.

M/A-COM's AM42-0040 is fabricated using a mature 0.5 micron GaAs MESFET process. The process features full chip passivation for increased performance and reliability. These amplifiers are 100% RF tested to ensure compliance to performance specifications.



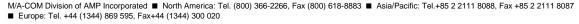
 $.XX = \pm 0.010$ 

### **Ordering Information**

Part Number	Package	
AM42-0040	Ceramic Bolt Down Package	

## **Electrical Specifications:** $T_A = +25^{\circ}C$ , $V_{DD} = +9V$ , $V_{GG}$ adjusted for $I_{DD} = 1050$ mA, Frequency = 5.9 to 6.4 GHz

Parameter	Abbv.	Test Conditions	Units	Min.	Тур.	Max.
Linear Gain	GL	P <sub>IN</sub> ≤ -10 dBm	dB	27	30	_
Input VSWR	VSWR <sub>IN</sub>	P <sub>IN</sub> ≤ -10 dBm	—	—	2.3:1	2.7:1
Output VSWR	VSWR <sub>OUT</sub>	P <sub>IN</sub> ≤ -10 dBm	—	—	3.0:1	—
Output Power	P <sub>SAT</sub>	$P_{IN}$ = +10 dBm, $I_{DD}$ =1050 mA Typ.	dBm	31.7	33.0	34.3
Output Power vs. Frequency	P <sub>SAT</sub>	$P_{IN}$ = +10 dBm, $I_{DD}$ =1050 mA Typ.	dB	—	1.0	1.5
Output Power vs. Temperature	P <sub>SAT</sub>	$P_{IN}$ = +10 dBm, $I_{DD}$ =1050 mA Typ.	dB	—	±0.4	_
(with respect to $T_A = +25^{\circ}C$ )		$T_A$ = -40°C to +70°C				
Drain Bias Current	I <sub>DD</sub>	$P_{IN} = +10 \text{ dBm}$	mA	900	1050	1100
Gate Bias Voltage	V <sub>GG</sub>	$P_{IN}$ = +10 dBm, $I_{DD}$ =1050 mA Typ.	V	-2.4	-1.2	-0.4
Gate Bias Current	I <sub>GG</sub>	$P_{IN}$ = +10 dBm, $I_{DD}$ =1050 mA Typ.	mA	—	5	20
Thermal Resistance	$\theta_{\text{JC}}$	25°C Heat Sink	°C/W	—	5.6	—
Second Harmonic	f <sub>2</sub>	$P_{IN}$ = +10 dBm, $I_{DD}$ =1050 mA Typ.	dBc	—	-35	_
Third Harmonic	f <sub>3</sub>	$P_{IN}$ = +10 dBm, $I_{DD}$ =1050 mA Typ.	dBc	_	-45	_





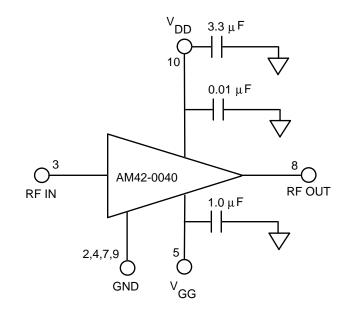
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## Absolute Maximum Ratings<sup>1,2,3,4</sup>

Parameter	Absolute Maximum			
Input Power	+23 dBm			
V <sub>DD</sub>	+12 Volts			
V <sub>GG</sub>	-3 Volts			
V <sub>DD</sub> - V <sub>GG</sub>	12 Volts			
I <sub>DD</sub>	1700 mA			
Channel Temperature	-40°C to +85°C			
Storage Temperature	-65°C to +150°C			

- 1. Exceeding any one or a combination of these limits may cause permanent damage.
- 2. Case Temperature  $(T_c) = +25^{\circ}C$ .
- 3. Nominal bias is obtained by first connecting -2.4 volts to pin 5 (V<sub>GG</sub>), followed by connecting +9 volts to pin 10 (V<sub>DD</sub>). Note sequence. Adjust V<sub>GG</sub> for a drain current of 1050 mA typical.
- 4. RF ground and thermal interface is the flange (case bottom). Adequate heat sinking is required.
- 5. No dc supply voltage will appear at the RF ports.
- 6. The dc resistance at the input and output ports is a short circuit. No voltage is allowed on these ports.
- 7. For optimum IP<sub>3</sub> performance, the  $V_{DD}$  bypass capacitors should be placed within 0.5 inches of the  $V_{DD}$  leads.

## **Typical Bias Configuration**<sup>4,5,6,7</sup>



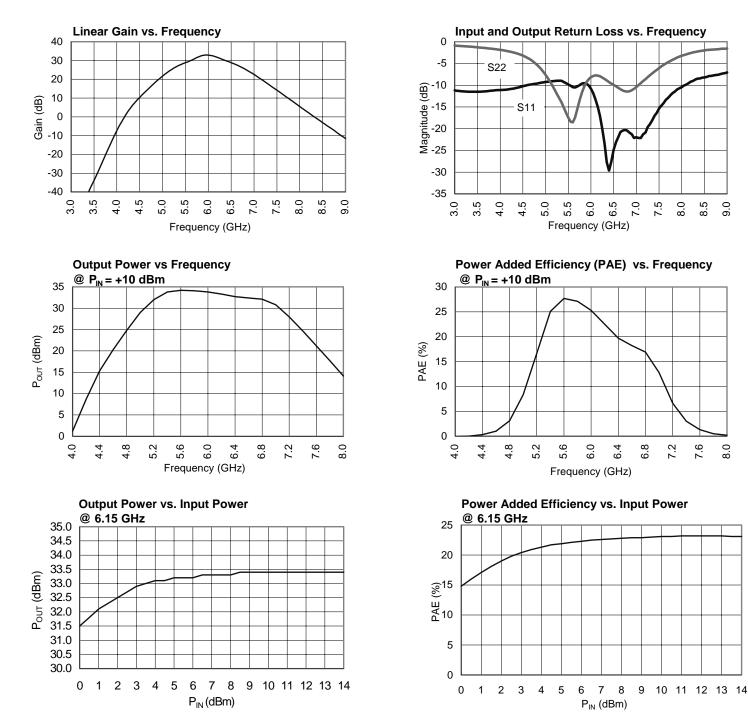
### **Pin Configuration**

Pin No.	Pin Name	Description
1	N/C	No Connection
2	GND	DC and RF Ground
3	RF In	RF Input
4	GND	DC and RF Ground
5	V <sub>GG</sub>	Gate Supply
6	N/C	No Connection
7	GND	DC and RF Ground
8	RF Out	RF Output
9	GND	DC and RF Ground
10	V <sub>DD</sub>	Drain Supply

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## Typical Performance @ +25°C





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